AN MOS/LSI ANALOG-TO-DIGITAL CONVERTER

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SUMMARY

The design and performance of a monolithic metal oxide semiconductor (MOS) analog-to-digital (A/D) converter are described. The converter accepts input voltages of ± 5 volts, has a 10-bit resolution including sign, operates at approximately 40 kHz, and utilizes MOS operational amplifiers.

INTRODUCTION

This paper describes the design of a monolithic analog-to-digital converter using p-channel enhancement mode technology. The converter, which utilizes a charge division method for digitizing, is composed of four basic functions; namely, a capacitance switching network, an integrating amplifier, a voltage comparator, and a digital control section. (See Figures 1 and 2.)

ANALOG-TO-DIGITAL CONVERTER

The operation of the converter is based upon the successive division of a charge proportional to the analog input between two equal (within the conversion accuracy) capacitors, and its subsequent integration with a charge proportional to a reference voltage. The polarity of an integrating amplifier output, after one half of each bit time of the conversion, is sensed

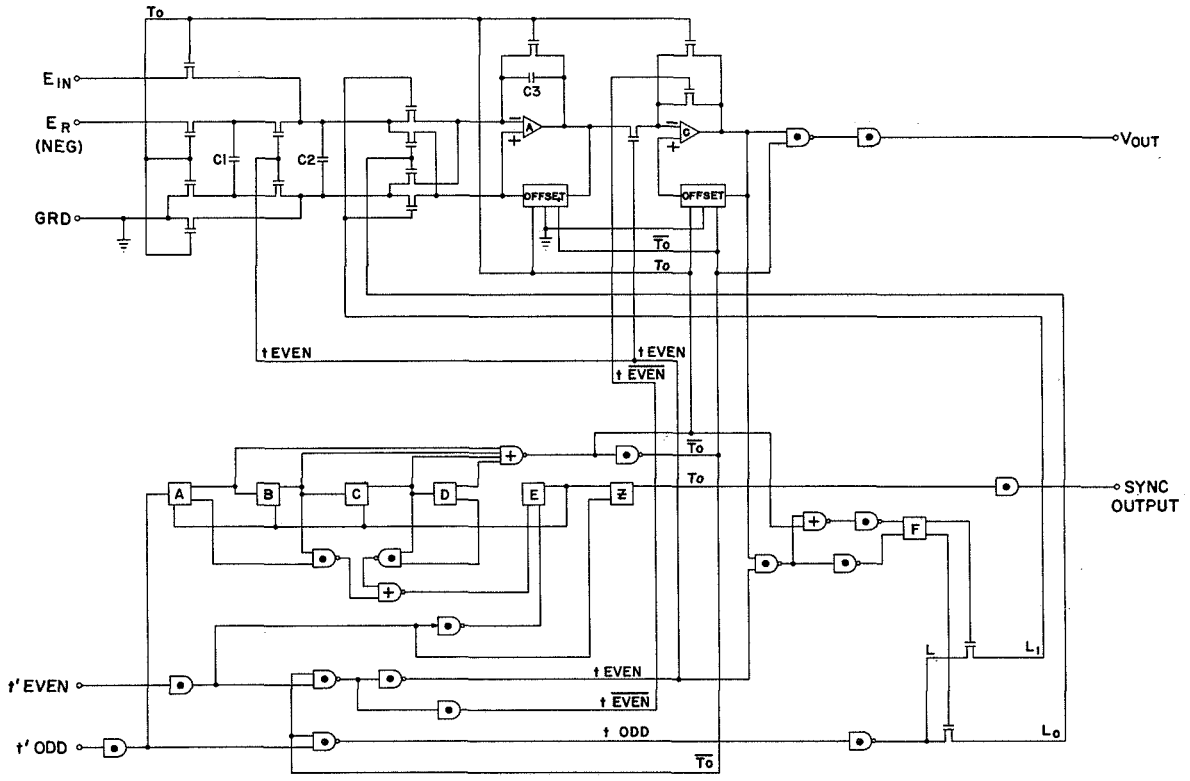

Figure 1. Analog-to-digital converter MOS/LSI.

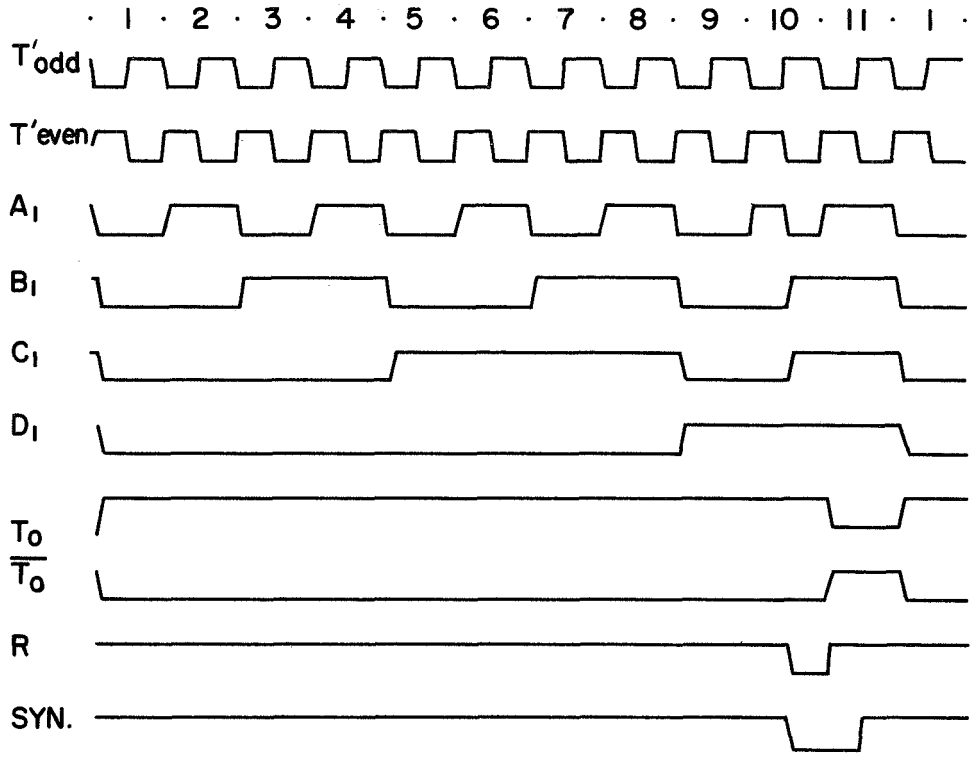

Figure 2. Analog-to-digital converter clock and control logic phasing.

by a voltage comparator and represents first the sign and subsequently the presence of a binary 1 or 0.

The MOS capacitors used in the capacitance switching network employ p-n junction isolation and are precisely balanced topologically and schematically to offset the effect of switching transients and parasitic capacitances.

A single operational amplifier configuration is used for both the integrating amplifier and voltage comparator functions. The amplifier design employs three successive differential stages and current mode feedback to minimize the effect of supply voltage and MOS device parameter variations on amplifier performance and operating point. Also, a dynamic offset and drift correction scheme is utilized wherein the amplifier is operated in a unity gain mode for one bit time between conversions. Its output is sampled, stored on a capacitor, and subsequently added to the amplifier input during normal operation so as to buck out any offset or drift voltage.

The control section of the converter divides and operates on a two-phase pulse input, whose frequency is eleven times the conversion rate, to produce the necessary timing and control signals used in the converter operation.

The design goals for the monolithic MOS analog-to-digital converter are as follows:

Resolution	10 bits including sign
Code	Binary using sign magnitude representation
Conversion Rate	40 000 per second
Range	±5.00 volts full scale
Output Logic Levels	0, -20 volts
Accuracy	0.05 percent ±1/2 LSB @ 298.15°K (25°C)
Stability	0.005 percent per 90 days
Temperature Coefficient	0.001 percent per 274.15°K (1°C) (worst case)

The converter will occupy a chip area of approximately 30.48×10^{-4} by 30.48×10^{-4} meter (120 by 120 mils). Supply voltage requirements are -27 volts and +12 volts, both ±1 percent, and +5.12 volts, ±0.1 percent. Power dissipation will be less than 200 milliwatts. Initial packaging plans call for the use of a round 0.953 cm (0.375 inch) diameter 22-lead flatpack that will allow for the availability of a number of internal test points in addition to the required pins.